SPECIFICATION

[Title of the Invention]

Integrated Circuit Having Memory Cell Array Configuration Capable of Simultaneously Performing Data Read Operation and Data Write Operation

[Brief Description of the Drawings]

FIG. 1 is a timing diagram illustrating an operation of a memory device having separate IOs;

FIG. 2 is a block diagram illustrating a structure of an integrated circuit (IC) according to the present invention;

FIG. 3 is a flowchart illustrating a method of simultaneously performing data read and write operations using the integrated circuit (IC) shown in FIG. 2;

FIG. 4 is a flowchart illustrating process 340 shown in FIG. 3;

FIG. 5 is a flowchart illustrating process 345 shown in FIG. 3;

FIG. 6 is a flowchart illustrating process 355 shown in FIG. 3;

FIG. 7 is a block diagram illustrating a structure of a memory of the IC according to the present invention; and

FIG. 8 illustrates mapping of a sub-memory block and a data memory block.

[Detailed Description of the Invention]

[Object of the Invention]

[Technical Field of the Invention and Related Art prior to the Invention]

The present invention relates to an integrated circuit (IC), and more particularly, to an integrated circuit (IC) which has a memory cell array configuration capable of simultaneously performing a data read operation and a data write operation.

A general synchronous RAM can transmit either read data or write data during each period of a clock signal.

A double data rate RAM increases a data transmission rate by transmitting data at both a rising edge and a falling edge of a clock signal. However, in a conventional memory device, data input and data output are performed via one pin. When using a common IO, data input and data output cannot be independently controlled. Thus, an input frequency and output frequency of data are limited.

However, as the bandwidth of a memory device becomes important, products using separate IOs have been manufactured. In other words, an input pin and an

output pin are separate so that data input and data output are independently controlled. A memory device having separate input and output pins can receive a read command, a read address, a write command, a write address, and write data within one period of a clock signal, and thus can increase operating frequency.

However, when a memory device having separate IOs receives a read command, a read address, a write command, a write address, and write data within one period of a clock signal, memory cell accesses should be performed twice so that a data read operation and a data write operation are performed within one period of a clock signal.

In other words, since the activation of a word line for data reading and data writing should be performed twice within one period of a clock signal, the clock frequency is limited by the activation time of a word line.

FIG. 1 is a timing diagram illustrating an operation of a memory device having separate IOs.

Since the relation between an address and a word line or the latency of input data and output data vary according to the structure of a circuit of the memory device, such a relation or latency is not considered in FIG. 1.

Referring to FIG. 1, a write address WADD and a read address RADD are input within one period of a clock signal CLK. Addresses A0, A2, A4, and A6 input at a rising edge of the clock signal CLK are read addresses RADDs, and addresses A1, A3, A5, and A7 input at a falling edge of the clock signal CLK are write addresses WADDs.

A read selection signal RES is used to select a read address RADD, and a write selection signal WES is used to select a write address WADD, respectively.

A word line AWL0 for data reading and a word line AWL1 for data writing should be activated within one period of the clock signal CLK. Thus, one period of the clock signal cannot be shorter than the activation time of a word line.

[Technical Goal of the Invention]

The present invention provides an integrated circuit (IC) having a memory cell array configuration capable of simultaneously performing data read and write operations so that a period of a clock signal is reduced.

[Structure and Operation of the Invention]

According to one aspect of the present invention, there is provided an

integrated circuit to which IOs are separately provided and to which a write address and a read address are simultaneously input during one period of a clock signal, the integrated circuit comprising a plurality of memory blocks, each of the memory blocks having a plurality of sub-memory blocks; data memory blocks corresponding to the memory blocks; and a tag memory controlling unit, which writes data in the memory blocks or reads the data from the memory blocks in response to the write address or the read address, wherein even though the simultaneously-input write address and read address are the same, access to the same sub-memory block is not simultaneously performed.

The sub-memory blocks may be a set of memory cells for sharing a common word line or bit line. In the sub-memory blocks, two or more word lines or bit lines cannot be simultaneously activated. Each of the data memory blocks may have the same size as the size of one sub-memory block.

If each of the data memory block has the same size as the size of one sub-memory block, the data memory block may have the number of columns and rows different from the number of columns and rows of the sub-memory block. The tag memory controlling unit may have the same number of decoding addresses as the number of addresses for decoding the data memory blocks.

The tag memory controlling unit may have the number of columns and rows different from the number of columns and rows of each of the data memory blocks.

The tag memory controlling unit may store a data memory address indicating that data being currently stored in the data memory block is originally data corresponding to a sub-memory block, and valid determination information on determining whether data being currently stored in the data memory block is valid.

If the number of the sub-memory blocks is 2^N, each address of the tag memory controlling unit may include N+1 data bits, and N-bit of the N+1 data bits may indicate a data memory address, and remaining 1-bit of the N+1 data bits may indicate the valid determination information.

The data memory blocks may have a direct mapping relation with the sub-memory blocks. The data may be input or output at a single data rate (SDR) or a double data rate (DDR).

Hereinafter, the present invention will be described in detail by describing exemplary embodiments of the invention with reference to the accompanying drawings. Like reference numerals refer to like elements throughout the drawings.

FIG. 2 is a block diagram illustrating a structure of an integrated circuit (IC) according to the present invention. Referring to FIG. 2, an integrated circuit (IC) 200 includes memory blocks MB1, MB2, MB3, and MB4, each of the memory blocks having a plurality of sub-memory blocks SMB1, SMB2, SMB3, . . . ,SMB M-1, and SMB M, data memory blocks DMB1, DMB2, DMB3, and DMB4 corresponding to the memory blocks MB1, MB2, MB3, and MB4, and a tag memory controlling unit 210. In the integrated circuit (IC) 200 shown in FIG. 2, IOs (not shown) are separate, and a write address WADD and a read address RADD are input during one period of a clock signal.

The memory blocks MB1, MB2, MB3, and MB4 have the same structure, and the data memory blocks DMB1, DMB2, DMB3, and DMB4 have the same structure. Thus, a second memory block MB2 among the memory blocks MB1, MB2, MB3, and MB4 and a second data memory block DMB2 among the data memory blocks DMB1, DMB2, DMB3, and DMB4 will be described below.

Each of the write address WADD and the read address RADD is divided into an upper address and a lower address. The upper address is an address that defines one selected from a plurality of sub-memory blocks.

In the present invention, basically, when the write address WADD and the read address RADD are the same, a data read operation and a data write operation are simultaneously performed in each of a memory block and a data memory block so that a period of a clock signal is reduced.

In other words, when the write address WADD and the read address RADD are the same and the data write operation and the data read operation should be simultaneously performed in one sub-memory block (e.g., SMB2), if the data read operation is performed in the sub-memory block SMB2, the data write operation is performed in the data memory block DMB2 corresponding to the sub-memory block SMB2.

Conversely, if the data write operation is performed in the sub-memory block SMB2, the data read operation is performed in the data memory block DMB2 corresponding to the sub-memory block SMB2. In this manner, the data read operation and the data write operation can be performed simultaneously and in parallel, and a period of a clock signal can be reduced.

To this end, a predetermined memory cell of the sub-memory block SMB2 is direct-mapped to a predetermined memory cell of the data memory block DMB2. In

addition, the data write operation and the data read operation may be continuously performed in the same sub-memory block. Thus, the size of a data memory block should be the same as or larger than the size of a sub-memory block.

The tag memory controlling unit 210 determines whether either the data write operation or the data read operation is performed in one of the sub-memory block and the data memory block. The tag memory controlling unit 210 reads data stored in the memory blocks MB1, MB2, MB3, and MB4 and the data memory blocks DMB1, DMB2, DMB3, and DMB4 or writes data in the memory blocks MB1, MB2, MB3, and MB4 and the data memory blocks DMB1, DMB2, DMB3, and DMB4 in response to the write address WADD or the read address RADD.

When the write address WADD is the same as the read address RADD and the data read operation is performed in one sub-memory block of the memory block MB2 and the data write operation is performed in the data memory block DMB2, an address of the sub-memory block SMB2 in which the data written in the data memory block DMB2 should be originally written, is stored in the tag memory controlling unit 210 as a data memory address.

In other words, the data memory address is an upper address that defines a sub-memory block in which the data stored in the data memory block DMB2 should be originally stored.

In order to recognize the data memory address stored in the tag memory controlling unit 210, the position of the data memory address stored in the tag memory controlling unit 210 can be known using a lower address among input addresses.

When a next write address WADD is the same as a next read address RADD and the previous write address WADD is the same as the previous read address RADD, the data write operation should be performed again in the data memory block DMB2. In this case, whether data written first in the data memory block DMB2 is valid data should be determined.

If it is determined that the data is valid data, the data written first in the data memory block DMB2 is read and written in a sub-memory block corresponding to the memory block MB2, and data corresponding to the next write address WADD should be written in the data memory block DMB2. Validity determination information obtained by determining whether the data stored in the data memory block DMB2 is valid, is stored in the tag memory controlling unit 210.

In addition, when the write address WADD is different from the read address RADD, two different sub-memory blocks corresponding to both the write and read addresses WADD and RADD are each decoded.

To this end, in the IC 200, a write address decoding path (not shown) and a read address decoding path (not shown) should be separate. The sub-memory blocks SMB1, SMB2, SMB3, . . . , SMB M-1, and SMB M should be connected to each of the write address decoding path and the read address decoding path.

Data is input or output via an input pin or an output pin at a single data rate (SDR) or a double data rate (DDR).

FIG. 3 is a flowchart illustrating a method of simultaneously performing a data read operation and a data write operation using the integrated circuit (IC) shown in FIG. 2.

First, in process 310, it is determined whether both a write address and a read address are input or either the write address or the read address is input during one period of a clock signal.

The tag memory controlling unit 210 receives a write address WADD and a read address RADD. If both the write address WADD and the read address RADD are input during one period of a clock signal, in process 320, it is determined whether an upper address of the write address WADD is the same as an upper address of the read address RADD.

The write address WADD or the read address RADD has information used to define a sub-memory block in upper bits. Thus, if the write address WADD or the read address RADD is input, the upper address of the write address WADD or the read address RAD is recognized, and it is determined what sub-memory block is defined.

If the upper address of the write address WADD is the same as the upper address of the read address RADD, in process 330, it is determined whether the write address WADD and the read address RADD are the same as a predetermined data memory address.

If the upper address of the write address WADD is the same as the upper address of the read address RADD, the write address WADD and the read address RADD define the same sub-memory block. In this case, one of a data write operation or a data read operation should be performed in a sub-memory block, and the other operation should be performed in a data memory block.

The tag memory controlling unit 210 stores a data memory address. The data memory address represents an address of a sub-memory block corresponding to the data memory block DMB2. If the write address WADD is the same as the data memory address, the data write operation should be performed in the data memory block DMB2.

If any one of the write address WADD and the read address RADD is not the same as the data memory address, in process 340, the data read operation is performed in the sub-memory block corresponding to the read address RADD, and the data write operation is performed in the data memory block.

Process 340 will be described in greater detail with reference to FIG. 4. If any one of the write address WADD and the read address RADD is not the same as the data memory address, in process 410, it is determined whether data stored in the data memory block is valid.

The fact that one of the write address WADD and the read address RADD is not the same as the data memory address means that the data read operation and the data write operation should be performed in the sub-memory block of the memory block MB2. However, a write word line and a read word line cannot be simultaneously enabled in the same sub-memory block. Thus, the data memory block DMB2 is used.

If the data stored in the data memory block is not valid, in process 440, the data read operation is performed in the sub-memory block corresponding to the read address, and the data write operation is performed in the data memory block.

When the data write operation and the data read operation are performed in the same sub-memory block, the data read operation is first performed. Thus, the data read operation is performed in the sub-memory block of the memory block MB2 corresponding to the read address RADD. Since the data stored in the data memory block DMB2 is not valid, the data write operation is performed in the data memory block DMB2.

Since the data stored in the data memory block DMB2 is changed by a new data write operation, in process 450, information on the data written in the data memory block is updated. Updating of the information is performed by the tag memory controlling unit 210.

If the data stored in the data memory block is valid, in process 420, the data read operation is performed in the sub-memory block corresponding to the read

address, and the valid data stored in the data memory block is read and written in the corresponding sub-memory block.

When the data write operation and the data read operation are performed in the same sub-memory block, the data read operation is first performed, and thus, the data read operation is performed in the sub-memory block of the memory block MB2 corresponding to the read address RADD.

Since the data stored in the data memory block DMB2 is valid data, the valid data stored in the data memory block DMB2 should be read, and the read data should be written in the corresponding sub-memory block of the memory block.

In process 430, a new data write operation is performed in the data memory block DMB2, and information on the data written in the data memory block DMB2 is updated. Updating of the information is performed by the tag memory controlling unit 210.

The data write operation and the data read operation are simultaneously performed. In other words, since the data write operation and the data read operation are independently performed in the sub-memory block and the data memory block DMB2, the write word line and the read word line can be simultaneously enabled.

Thus, the write word line and the read word line are sequentially enabled such that the period of a clock signal is not limited.

If the write address or the read address is coincident with the data memory address in process 330, in process 345, it is determined whether only one of the write address and the read address is coincident with the data memory address or both the write address and the read address are coincident with the data memory address, and the data write operation and the data read operation are performed.

Process 345 will be described in greater detail with reference to FIG. 5. If only one of the write address and the read address is coincident with the data memory address, in process 510, an operation corresponding to an address coincident with the data memory address is performed in the data memory block, and an operation corresponding to an address not coincident with the data memory address is performed in the sub-memory block.

In other words, if the read address RADD is coincident with the data memory address and the write address WADD is not coincident with the data memory address, the data read operation is performed in the data memory block DMB2.

Conversely, if the write address WADD is coincident with the data memory address and the read address RADD is not coincident with the data memory address, the data write operation is performed in the data memory block DMB2, and the data read operation is performed in the memory block MB2.

If both the write address and the read address are not coincident with the data memory address, in process 520, the data read operation is performed in the data memory block, the data write operation is performed in the sub-memory block, and information on the data written in the sub-memory block is updated.

If both the write address and the read address are coincident with the data memory address, the data write operation and the data read operation should be performed in the data memory block DMB2.

However, this is not possible because the data write operation and the data read operation cannot be simultaneously performed in the same sub-memory block. Thus, the data read operation is performed in the data memory block DMB2. The data write operation is performed in the corresponding sub-memory block of the memory block MB2.

Since the data to be originally written in the data memory block DMB2 is written in the sub-memory block, the data being currently stored in the data memory block DMB2 is not valid data. Thus, the information is updated by the tag memory controlling unit 210.

In process 320, if the upper address of the write address is not the same as the upper address of the read address, in process 350, it is determined whether the write address and the read address are coincident with the data memory address.

In process 355, it is determined whether one of the write address and the read address is coincident with the data memory address or both the write address and the read address are coincident with the data memory address, and the data write operation and the data read operation are performed.

Process 355 will be described in greater detail with reference to FIG. 6. If any one of the write address and the read address is coincident with the data memory address, in process 610, an operation corresponding to an address coincident with the data memory address is performed in the data memory block, and an operation corresponding to an address not coincident with the data memory address is performed in the sub-memory block.

In other words, if the read address RADD is coincident with the data memory address and the write address WADD is not coincident with the data memory address, the data read operation is performed in the data memory block DMB2. In addition, the tag memory controlling unit 210 performs the data write operation in the sub-memory block.

Conversely, if the write address WADD is coincident with the data memory address and the read address RADD is not coincident with the data memory address, the data write operation is performed in the data memory block DMB2, and the data read operation is performed in the sub-memory block.

If both the write address and the read address are coincident with the data memory address, in process 620, the data read operation is performed in the data memory block, the data write operation is performed in the sub-memory block, and information on the data written in the sub-memory block is updated.

If both the write address and the read address are coincident with the data memory address, the data write operation and the data read operation should be performed in the data memory block DMB2.

However, this is because the data write operation and the data read operation cannot be simultaneously performed in the same sub-memory block. Thus, the data read operation is performed in the data memory block DMB2. The data write operation is performed in the corresponding sub-memory block of the memory block MB2.

Since the data to be originally written in the data memory block DMB2 is written in the sub-memory block, the data being currently stored in the data memory block DMB2 is not valid data. Thus, the information is updated by the tag memory controlling unit 210.

As a determination result in process 350, if both the write address and the read address are not coincident with the data memory address, in process 360, a data write operation and a data read operation are performed in different sub-memory blocks corresponding to the write address and the read address among the selected memory blocks.

In this case, the write address WADD and the read address RADD define different sub-memory blocks. Since the different sub-memory blocks are defined, a data read operation and a data write operation are performed using a decoding circuit (not shown) corresponding to each sub-memory block.

In process 310, if any one of the write address and the read address is input, in process 365, it is determined whether one of the write address and the read address is coincident with the data memory address.

If the input write address or read address is coincident with the data memory address, in process 370, an operation corresponding to the write address or read address coincident with the data memory address is performed in the data memory block.

In this case, only one of the write address WADD and the read address RADD is input during one period of a clock signal. If the input address is coincident with the data memory address, the operation corresponding to the data memory block is performed, and if the input address is not coincident with the data memory address, the operation corresponding to the sub-memory block is performed.

In other words, if only the write address WADD is input and the input write address WADD is coincident with the data memory address, the data write operation is performed in the data memory block DMB2.

Conversely, if only the read address RADD is input and the input read address RADD is coincident with the data memory address, the data read operation is performed in the data memory block DMB2.

If the input write address or read address is not coincident with the data memory address, in process 375, an operation corresponding to the write address or read address not coincident with the data memory address is performed in the sub-memory block.

The internal operation of the IC for performing a data read operation and a data write operation has been described with reference to FIGS. 2 through 6. A structure of a sub-memory block, a data memory block, and a tag memory controlling unit for performing the internal operation of the IC will be described below.

FIG. 7 is a block diagram illustrating a structure of a memory of the IC according to the present invention. In FIG. 7, the tag memory controlling unit 210 is excluded from the block diagram of FIG. 2. In other words, memory blocks MAT A, MAT B, MAT C, and MAT D of FIG. 7 correspond to memory blocks MB1, MB2, MB3, and MB4 of FIG. 2.

The memory blocks MAT A, MAT B, MAT C, and MAT D include cells in which all of data defined in specification of a memory is stored, and a plurality of sub-memory blocks (see a second memory block MB2 of FIG. 2).

Even though simultaneously-input write address and read address are the same, access to the same sub-memory block is simultaneously not performed. Specifically, two or more word lines or bit lines cannot be simultaneously activated in the same sub-memory block.

This is because, if two or more word lines or bit lines are simultaneously activated in the same sub-memory block, a data write operation or a data read operation is performed on a plurality of cells in one sub-memory block.

Sub-memory blocks may be a set of memory cells for sharing a common word line so that two or more word lines or bit lines are not simultaneously activated. Alternatively, sub-memory blocks may be a set of memory cells for sharing a common bit line so that two or more word lines or bit lines are not simultaneously activated.

Each sub-memory block includes a plurality of IOs. If the number of IOs of the IC is 36 and one sub-memory block includes nine IOs, four sets of sub-memory blocks are needed, as shown in FIG. 7. A set of sub-memory blocks is referred to as MAT, for convenience sake.

In FIG. 7, one MAT includes a plurality of sub-memory blocks. The number of IOs output from one MAT is nine. A plurality of sub-memory blocks of one MAT are connected to each of nine IOs.

One data memory block corresponds to one MAT. The size of a data memory block is the same as the size of one sub-memory block. For example, if one MAT includes 16 sub-memory blocks, the size of a data memory block is 1/16 of the size of one MAT.

Since four MATs and four data memory blocks exist in the IC of FIG. 7, the size of a data memory block is 1/16 of the size of a memory block, i.e., four MATs, existing in the IC.

That a data memory block has the same size as that of one sub-memory block is because a data write operation and a data read operation cannot be simultaneously performed in one sub-memory block, in preparation for a case where the data write operation and the data read operation are simultaneously performed in a sub-memory block.

In addition, a data memory block has the same size as that of one sub-memory block such that determination on a comparison operation and an internal operation of a tag memory controlling unit can be quickly performed.

FIG. 8 illustrates mapping of a sub-memory block and a data memory block.

If the data memory block has the same size as that of one sub-memory block, the data memory block may have the number of columns and rows different from the number of columns and rows of the sub-memory block.

For example, assuming that the sub-memory block includes 32 columns, 512 rows, and 9 IOs, the number of cells contained in one sub-memory block is expressed as 32 x 512 x 9 = 147,456. 512 cells are connected to one bit line such that a cell access time increases.

Thus, since the size of a cell array of the data memory block is not large, in the data memory block, 512 rows are changed into 64 rows, an address of the sub-memory block corresponds to an address of the data memory block using direct address mapping so that an access time of the data memory block can be reduced.

In the memory blocks MAT A, MAT B, MAT C, and MAT D having sub-memory blocks, due to the limitation of the size of the IC or an aspect ratio of the IC, it is difficult to change the number of columns and rows of one sub-memory block arbitrarily only for improvement of the cell access time.

However, since the area of the data memory block in the IC is small, re-mapping of an address is possible so that the data memory block has an optimum cell access time.

In FIG. 8, since the sub-memory block includes 512 rows and 32 columns, the sub-memory block includes 9 row addresses ($512 = 2^9$) and 5 column addresses ($32 = 2^5$).

If the data memory block is re-mapped, it is divided into 8 small blocks, the number of row addresses is 6 ($64 = 2^6$), and remaining 3 row addresses may be used as a block selection signal used to select 8 small blocks.

This is just one example. In this way, a variety of mapping methods may be used according to a structure of MAT having sub-memory blocks and a cell access time required for a data memory block.

The tag memory controlling unit stores a data memory address indicating that data being currently stored in the data memory block is originally data corresponding to a sub-memory block, and valid determination information on determining whether data being currently stored in the data memory block is valid.

Thus, the space of the address occupied by the tag memory controlling unit is one sub-block, like in the data memory block, and the IC having no function of

separately writing for each IO such as byte-write, has only to include one tag memory controlling unit.

However, when the IC has the function of byte-write, the contents of the data memory block are varied by byte, the IC should include a tag memory controlling unit for each byte.

The tag memory controlling unit has the same number of decoding addresses as the number of addresses for decoding the data memory block. However, the tag memory controlling unit may have the number of columns and rows different from the number of columns and rows of the data memory block.

In other words, the tag memory controlling unit can perform re-mapping, like in the data memory block, if a cell access time is required.

There is only a difference in re-mapping that in the data memory block, data corresponding to one address of the sub-memory block is IO data, whereas the tag memory controlling unit includes address data corresponding to the data memory address and valid bits corresponding to the valid determination information.

If the number of sub-memory blocks is 2^N, each address of the tag memory controlling unit includes N+1 data bits. N-bit of the N+1 data bits indicates a data memory address, and remaining 1-bit of the N+1 data bits indicates the valid determination information.

For example, if one MAT includes 32 sub-memory blocks (in a case where N = 5), each address of the tag memory controlling unit includes 6 data bits, and the number of address data indicating the data memory address is 5, and the number of valid bits indicating the valid determination information is 1.

While this invention has been particularly shown and described with reference to a preferred embodiment thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention as defined by the appended claims and equivalents thereof.

[Effect of the Invention]

As described above, in the integrated circuit (IC) having a memory cell configuration according to the present invention, a data read operation and a data write operation are simultaneously performed during one period of a clock signal, such that a period of the clock signal is reduced.